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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/792,112	03/03/2004	Mehmet Aslan	08211/0200382-US0/P05805	3898

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EXAMINER	
LE, JOHN H	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/792,112	ASLAN ET AL.	
	Examiner	Art Unit	
	John H. Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-19* is/are allowed.

6)☒ Claim(s) *1,3,5 and 20* is/are rejected.

7)☒ Claim(s) *2,4 and 6-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/16/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 5, 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kunst (USP 6,008,685).

Regarding claim 1, Kunst discloses a temperature measurement circuit (Fig.2), comprising: a temperature sensor circuit 200 that includes: a first current source circuit 215 (coupled to a first node), a second current source circuit 210 (coupled to a first node), two signal channels (s1, s2) that are configured to receive, at first and second sense nodes, a differential input signal from a dual junction temperature sensor circuit (200), and further configured to provide a differential intermediate signal from the differential input signal; two current source circuits (215, 210) configured to provide respective bias currents to the first and second sense nodes (see Fig.2, Col.2, lines 5-18); a conversion circuit that is configured to convert the differential intermediate signal into a digital temperature signal that is associated with a remote temperature (e.g. Col.4, lines 48-63, Col.5, lines 45-59); and a first multiplexer circuit (630) that is configured to control the differential intermediate signal (e.g. Fig.6, Col.8, lines 12-35).

Regarding claim 3, Kunst discloses the first multiplexer circuit (630) is configured to control the differential intermediate signal by multiplexing the two signal channels (e.g. Fig.6, Col.8, lines 12-35).

Regarding claim 5, Kunst discloses the multiplexer circuit (63) is configured to control the differential intermediate signal by multiplexing which one of the bias currents is-provided to which one of the two signal channels (e.g. Fig.6, Col.8, lines 12-35).

Regarding claim 20, Kunst discloses a temperature measurement circuit (Fig.2), comprising: a temperature sensor circuit 200 that includes: a first current source circuit 215 (coupled to a first node), a second current source circuit 210 (coupled to a first node), two signal channels (s1, s2) that are configured to receive, at first and second sense nodes, a differential input signal from a dual junction temperature sensor circuit (200), and further configured to provide a differential intermediate signal from the differential input signal; two current source circuits (215, 210) configured to provide respective bias currents to the first and second sense nodes (see Fig.2, Col.2, lines 5-18); a conversion circuit that is configured to convert the differential intermediate signal into a digital temperature signal that is associated with a remote temperature (e.g. Col.4, lines 48-63, Col.5, lines 45-59); means (a witch capacitor network) for substantially canceling at least one voltage offset that is included the means for providing (e.g. Col.10, lines 45-64, Col.13, lines 36-41).

Allowable Subject Matter

3. Claims 11-19 are allowed.

4. Claims 2, 4, 6-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 2, none of the prior art of record teaches or suggests the combination of a temperature measurement circuit, comprising: two signal channels that are configured to receive, at first and second sense nodes, a differential input signal from a dual Junction temperature sensor circuit, and further configured to provide a differential intermediate signal from the differential input signal; two current source circuits configured to provide respective bias currents to the first and second sense nodes; a conversion circuit that is configured to convert the differential intermediate signal into a digital temperature signal that is associated with a remote temperature; and a first multiplexer circuit that is configured to control the differential intermediate signal, wherein the conversion circuit includes a sigma-delta analog-to-digital converter circuit, and wherein the sigma-delta analog-to-digital converter circuit includes: an operational amplifier circuit; and a switched capacitor circuit that is responsive to a control signal, wherein the switched capacitor includes first and second capacitors, and wherein: if the control signal corresponds to the first logic level: the first capacitor is configured to operate as an integrator with positive gain, and the second capacitor is configured to operate as an integrator with negative gain; and if the control signal corresponds to the second logic level: the first capacitor

is configured to operate as an integrator with negative gain, and the second capacitor is configured to operate as an integrator with positive gain. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 4, none of the prior art of record teaches or suggests the combination of a temperature measurement circuit, comprising: two signal channels that are configured to receive, at first and second sense nodes, a differential input signal from a dual Junction temperature sensor circuit, and further configured to provide a differential intermediate signal from the differential input signal; two current source circuits configured to provide respective bias currents to the first and second sense nodes; a conversion circuit that is configured to convert the differential intermediate signal into a digital temperature signal that is associated with a remote temperature; and a first multiplexer circuit that is configured to control the differential intermediate signal, wherein the first multiplexer circuit is configured to control the differential intermediate signal by multiplexing the two signal channels; a first buffer circuit coupled between the first multiplexer circuit and the first sense node; and a second buffer circuit coupled between the first multiplexer circuit and the second sense node; and another multiplexer circuit that is coupled between the first and second sense nodes and the first and second buffer circuits. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been

found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 6, none of the prior art of record teaches or suggests the combination of a temperature measurement circuit, comprising: two signal channels that are configured to receive, at first and second sense nodes, a differential input signal from a dual Junction temperature sensor circuit, and further configured to provide a differential intermediate signal from the differential input signal; two current source circuits configured to provide respective bias currents to the first and second sense nodes; a conversion circuit that is configured to convert the differential intermediate signal into a digital temperature signal that is associated with a remote temperature; and a first multiplexer circuit that is configured to control the differential intermediate signal, wherein the multiplexer circuit is configured to control the differential intermediate signal by multiplexing which one of the bias currents is-provided to which one of the two signal channels; a control circuit that is configured to provide a first control signal such that the first control signal corresponds to a first logic level at a first time, and a second logic level at a second time, wherein the first multiplexer circuit is configured to receive a first control signal, and wherein the first multiplexer circuit is arranged such that multiplexing which one of the bias currents is provided to which one of the two signal channels is selected according to the first control signal, and wherein the differential intermediate signal includes a first differential voltage at the first time, and a second differential voltage at the second time. It is these limitations as they are claimed in the combination with other limitations of

claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 11, none of the prior art of record teaches or suggests the combination of a temperature measurement circuit, comprising: a control circuit that is configured to provide a current control signal; a sensing circuit that is configured to receive, at first and second sense nodes, a differential input signal from a dual junction temperature sensor circuit, and further configured to provide a differential intermediate signal from the differential input signal, wherein the sensing circuit includes: a first current source circuit that is configured to provide a first bias current, wherein the first bias current corresponds to one of a first value if the current control signal corresponds to a deasserted value, and corresponds to a second value if the current control signal corresponds to an asserted value; a second current source circuit that is configured to provide a second bias current such that the second bias current corresponds to a third value if the current control signal corresponds to the deasserted value, and corresponds to a fourth value if the current control signal corresponds to an asserted value, wherein the differential intermediate signal includes a differential voltage that depends at least in part on the current control signal; and a conversion circuit that is configured to convert the differential intermediate signal into a digital temperature signal that is associated with a remote temperature. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Contact Information

1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John H Le whose telephone number is 571-272-2275. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JL

John H. Le

Patent Examiner-Group 2863

July 21, 2005

MICHAEL NGHIE
PRIMARY EXAMI